

Raihan Fauzy Ferdyansyah

+62 813-5918-6578 | raihanfauzyferdyansyah@mail.ugm.ac.id | [linkedin.com/in/raihanfauzyferdyansyah](https://www.linkedin.com/in/raihanfauzyferdyansyah)

Profile

Biomedical Engineering graduate from Universitas Gadjah Mada focused on analog and mixed-signal IC design, especially low-voltage CMOS and data converters, with adjacent experience in engineering computation, data/ML, and industrial monitoring systems.

Technical Skills

IC Design & EDA	Cadence Virtuoso / Spectre, MATLAB, Xschem, ngspice, IIC-OSIC-TOOLS, KLayout, schematic simulation, corner analysis, physical layout
Programming & Data	Python, C/C++, SQL, LightGBM, scikit-learn, FastAPI, React
Embedded & Industrial Development	STM32, Modbus RTU/TCP, Node-RED, MySQL, InfluxDB, Grafana, sensor integration
	Git, Docker

Experience

Teaching Assistant - Basic Programming Laboratory Feb 2026 – Jun 2026
DTETI, Universitas Gadjah Mada

- Assisted undergraduate programming laboratories, guiding students through C/C++ fundamentals, algorithmic reasoning, debugging, and assignment review.

Engineering Intern Dec 2024 – Jan 2025
PT Mitra Ekatama Expertech (MEET)

- Configured Ebyte ME31 I/O and Modbus RTU/TCP communication. Built Node-RED status monitoring, MySQL logging, dashboard and Telegram notification paths.

Selected Projects

Third-Order Feedforward 3-Bit Sigma-Delta Modulator in 45-nm CMOS 2026
Undergraduate Thesis / IBIOMED 2026 Paper

- Reworked a published 180-nm, 1.8-V feedforward architecture for GPDK045 at 1.0 V using a PMOS-input folded-cascode OTA, bootstrapped switch, and resistive continuous-time CMFB.

Noise-included behavioral SNDR: mean 78.38 dB across 20 independent noise realizations, SD 0.23 dB. Feedback-DAC scaling is unspecified in the paper. This is not process or mismatch Monte Carlo.

- Checked closed-loop schematic transients and drew selected block-level layouts. Full-system PEX and transistor-level spectral SNDR were outside scope.

CMOS Schmitt Trigger - Chipathon 2026, Track B Ongoing
GF180MCU / Open-Source IC Flow

- Designed an 8-transistor CMOS Schmitt trigger in GF180MCU using Xschem/ngspice; characterized 5 process corners across 3 temperatures with hysteresis above 0.71 V and center-voltage variation within 140 mV.

Early Warning Karhutla - 7-Day Hotspot Risk, Riau 2026
Team Project - Modeling & Dashboard Development

- Developed/evaluated per-cell hotspot-risk models for Riau on a 5 km x 5 km grid and helped build a dashboard for a seven-day target window. Semifinalist, University Track DATATHON 2026, RISTEK Fasilkom UI.

Leadership & Recognition

- Software Division Lead, BIONCE** - DTETI UGM, 2025–2026.
- EMMA Smart Composting** - co-creator of registered software copyright (DGIP No. 001397406), 2026.

Education

Universitas Gadjah Mada Completed Jul 2026
B.Eng. Biomedical Engineering - CGPA 3.09/4.00

Selected coursework: Fundamental Electronics, Biomedical Electronics, Digital Engineering, Microcontroller Systems, Signals and Systems, Sensors and Transducers.

Karhutla scope: per-cell risk classification over a seven-day window, with maps as derived visualizations. The linked dashboard is a demonstration and currently labels its data as simulated.