Raihan Fauzy Ferdyansyah

Analog & Mixed-Signal IC Design | Low-Voltage CMOS | Data Converters

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Biomedical Engineering graduate focused on analog and mixed-signal IC design, with hands-on work in low-voltage CMOS data converters, transistor-level simulation, corner analysis, and block-level custom layout work.

Education

Universitas Gadjah Mada Jul 2026

B.Eng. Biomedical Engineering | GPA: 3.09/4.00

Relevant coursework: Fundamental Electronics, Biomedical Electronics, Digital Engineering, Signals and Systems, Sensors and Transducers, Microcontroller Systems.

Technical Skills

Analog / Mixed-Signal: CMOS circuit design, data converters, switched-capacitor circuits, OTA design, comparator/switch design, DC/AC/transient analysis, corner analysis, custom layout

EDA / PDKs: Cadence Virtuoso, Spectre, MATLAB, Xschem, ngspice, KLayout, IIC-OSIC-TOOLS; GPDK045 and GF180MCU.

Programming / Engineering: Python, C/C++, SQL, Git, Docker; engineering data analysis and model evaluation.

Selected Technical Projects

Third-Order Feedforward 3-Bit Sigma-Delta Modulator, GPDK045 2026

Undergraduate Thesis; IBIOMED 2026 conference paper

- Reworked a published 180-nm, 1.8-V feedforward architecture for 45-nm CMOS at 1.0 V, replacing the telescopic OTA, plain sampling switch, and SC-CMFB with a PMOS-input folded-cascode OTA, bootstrapped switch, and resistive continuous-time CMFB to address reduced-voltage headroom and switch-threshold constraints.

Noise-included behavioral SNDR: mean 78.38 dB across 20 independent noise realizations, SD 0.23 dB. Feedback-DAC scaling is unspecified in the paper. This is not process or mismatch Monte Carlo.

- Simulated OTA: 47.6 dB gain, 13.0 MHz GBW, 89.4 deg phase margin. Checked schematic transients and drew block layouts. Full-system PEX and transistor-level spectral SNDR were outside scope.

CMOS Schmitt Trigger - Chipathon 2026, Track B 2026 - Ongoing

GF180MCU; Xschem / ngspice / open-source IC flow

- Designed and characterized an 8-transistor CMOS Schmitt trigger across 5 process corners and 3 temperatures, maintaining hysteresis above 0.71 V and center variation within 140 mV at 3.3 V across the evaluated conditions.

Four-Stage Discrete BJT Amplifier 2024

2N5550; LTspice / KiCad / PCB / bench measurement

- Took a cascaded amplifier from hand analysis through LTspice simulation and KiCad PCB implementation to bench validation, measuring 96.8 V/V voltage gain against an approximately 100 V/V design target.

Experience

Engineering Intern Dec 2024 - Jan 2025

PT Mitra Ekatama Expertech (MEET)

- Configured Ebyte ME31 I/O and Modbus communication. Built Node-RED status monitoring, MySQL logging, dashboard and Telegram notification paths.

Teaching Assistant - Basic Programming Laboratory Feb 2026 - Jun 2026

DTETI, Universitas Gadjah Mada

- Guided undergraduate students through C/C++ fundamentals, algorithmic reasoning, debugging, and assignment review in laboratory sessions.

Leadership & Recognition

- **Software Division Lead, BIONCE** - DTETI UGM, 2025-2026.
- **EMMA Smart Composting** - co-creator of registered software copyright, DGIP No. 001397406 (2026).