Design of a Third-Order Feedforward 3-bit Sigma-Delta Modulator in 45-nm CMOS for Low-Power Wearable Biomedical Applications

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***Abstract*—Wearable biomedical monitoring requires high-resolution data conversion under stringent power constraints. This work redesigns a third-order feedforward 3-bit sigma-delta ($\Sigma\Delta$) modulator from a 180-nm, 1.8-V reference implementation using the Cadence Generic 45-nm CMOS PDK at 1.0 V. Reduced headroom is addressed using a fully differential folded-cascode operational transconductance amplifier (OTA), Dessouky–Kaiser bootstrapped switches, and resistive continuous-time common-mode feedback (CT-CMFB). The quantization-noise-only behavioral model reaches 83.5 dB peak signal-to-noise-and-distortion ratio (SNDR) at an effective oversampling ratio of 64. A revised noise-included behavioral evaluation uses a coherent 3.271-kHz input for which the second- through seventh-order harmonics remain within the 25-kHz signal band; across 20 independent noise realizations it gives a mean SNDR of 78.38 ± 0.23 dB and 12.73-bit effective number of bits (ENOB). Closed-loop schematic-level transistor simulation gives approximately 40 μW of V_{DD}-powered core power. Including 6.25 μW dissipated by the two externally driven resistor-string ladders gives a modeled subtotal of 46.25 μW before on-chip bias/reference-generator overhead. Combining this subtotal with the behavioral ENOB gives a projected Walden figure of merit of 136.37 fJ/conversion-step. The behavioral ENOB remains above 12 bits, consistent with the adopted electrocardiogram (ECG)-oriented design benchmark, although the more stringent 80-dB design target is not fully achieved.**

***Index Terms*—sigma-delta modulator, 45-nm CMOS, folded-cascode OTA, bootstrapped switch, low-power, biomedical, wearable, noise shaping**

I. Introduction

Cardiovascular and neurological disorders create growing demand for continuous physiological monitoring [1]. Wearable devices record electrocardiogram (ECG) and electroencephalogram (EEG) signals under tight battery constraints [2]. For ECG specifically, wearable and high-resolution acquisition literature uses 12-bit nominal analog-to-digital converter (ADC) resolution as a practical benchmark: a recent wearable-ECG review discusses a minimum 12-bit resolution for amplitude detail [3], while a published wearable ECG processor integrates a 12-bit ADC [4]. Accordingly, 12-bit nominal resolution is adopted here as an ECG-oriented application benchmark rather than as a universal effective-number-of-bits (ENOB) requirement for all biomedical signals.

A. Problem Statement

The problem addressed here is the realization of a $\Sigma\Delta$ modulator operating from 1.0 V in a generic 45-nm complementary metal–oxide–semiconductor (CMOS) PDK over a 25-kHz bandwidth, with a modeled modulator-power budget below 50 μW. Beyond the adopted 12-bit ECG-oriented benchmark, a more stringent SNDR target of ≥ 80 dB (approximately 13-bit ideal-equivalent resolution) is imposed to provide about one bit, or 6 dB, of design margin for implementation losses. Resolution and power are conflicting objectives because amplifier gain, bandwidth, and sampling capacitance all cost current or area.

B. Existing Approaches and Their Limitation at 45 nm

For low-bandwidth biomedical applications, $\Sigma\Delta$ ADCs achieve high resolution through oversampling and noise shaping, which moves quantization noise outside the signal band for subsequent removal by digital decimation filtering, and which relaxes analog component accuracy requirements [5], [6]. Reported low-power $\Sigma\Delta$ modulators for biomedical use are therefore predominantly implemented in mature 130–180-nm nodes at supplies of 0.6–1.8 V [7], [8]. The design of Akçakaya and Dündar [8] is representative: a third-order feedforward modulator with a 3-bit quantizer in UMC 180-nm CMOS at 1.8 V, reporting a post-layout SNDR of 81.3 dB at 28.2 μW and a figure of merit (FoM) of 59 fJ/conversion-step at an oversampling ratio (OSR) of 64. That design relies on a telescopic-cascode operational transconductance amplifier (OTA), plain NMOS sampling switches, and switched-capacitor common-mode feedback (SC-CMFB).

C. Motivation for a Scaled Node

Two considerations motivate a more scaled process. First, co-integration with digital decimation and signal-processing blocks motivates implementation on a compatible scaled CMOS node, avoiding the need for separate process technologies.

Second, reducing the supply from 1.8 V to 1.0 V can reduce power, although the current required to maintain bandwidth and settling may offset part of this advantage. This work therefore investigates the architecture using the Cadence Generic 45-nm CMOS PDK (GPDK045) at a 1.0-V supply.

Migration is not, however, a matter of re-simulating the same circuits in a new kit. Three difficulties arise, all of them consequences of the reduced supply and the shorter channel rather than of the modulator topology. First, at $V_{DD} = 1.0$ V an NMOS switch handling a mid-supply signal has $V_{GS} = 0.5$ V, below the extracted threshold $V_{th,N} = 0.588$ V, and neither the sampling nor the SC-CMFB switches conduct. Second, a five-transistor telescopic stack does not fit within 1.0 V while preserving the output swing the loop requires. Third, short-channel effects such as drain-induced barrier lowering (DIBL) reduce intrinsic output resistance and hence achievable DC gain [9], [10].

D. Proposed Approach and Contribution

This paper presents a redesign of the third-order feedforward 3-bit $\Sigma\Delta$ modulator of [8] using GPDK045 at 1.0 V. Three circuit-level substitutions address the three limitations above: a folded-cascode OTA with a PMOS input pair replaces the telescopic OTA to recover output swing and input common-mode range; Dessouky–Kaiser bootstrapped switches [11] replace the plain switches so that the gate-source voltage of the sampling device is held near V_{DD} independently of the signal; and a resistive continuous-time common-mode feedback (CT-CMFB) circuit replaces the SC-CMFB, removing the switch-threshold constraint at the cost of a small static current. The feedforward loop filter and the 3-bit quantizer of [8] are retained.

The expected benefit is tolerance of reduced amplifier gain: because the feedforward path keeps the integrator outputs dominated by shaped quantization noise rather than by the input signal, sensitivity to finite OTA gain is examined with a simplified leakage model in Section IV-A. The design is compared with [8] and other reported low-power modulators in Section IV-E. No fabrication, parasitic extraction, or Monte Carlo analysis is claimed; the verification reported here is behavioral and schematic-level transistor simulation.

Section II describes the architecture and system-level analysis, Section III the circuit-level design, Section IV the simulation results, and Section V concludes.

II. Modulator Architecture and System-Level Analysis

A. System Architecture

Fig. 1 shows the top-level architecture: three cascaded switched-capacitor (SC) integrators, feedforward summation paths, a 3-bit flash quantizer, and a resistive feedback DAC. The input is forwarded directly to the summing node preceding the quantizer, which reduces the signal swing at the integrator outputs and relaxes the linearity and output-swing requirements of the operational transconductance amplifiers (OTAs) [12].

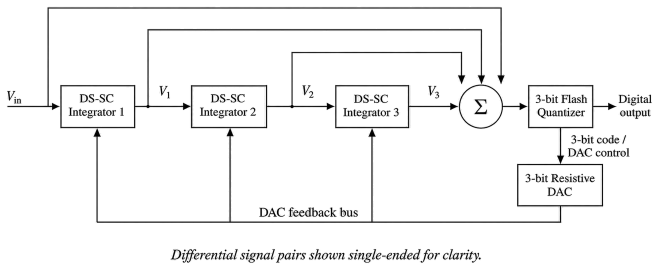

Fig. 1. Simplified architecture of the proposed third-order feedforward 3-bit $\Sigma\Delta$ modulator. Differential signal pairs are shown single-ended for clarity; the DAC feeds back to all three integrator stages.

For an L-th order modulator with an N-bit quantizer, the ideal signal-to-quantization-noise ratio (SQNR) is [5], [8]

$$\mathrm{SQNR}_{\mathrm{dB}} = 10\log_{10}\left[\frac{3}{2}\,\frac{2L+1}{\pi^{2L}}\,\mathrm{OSR}^{\,2L+1}\,2^{\,2(N-1)}\right]. \quad (1)$$

For $L = 3$, $N = 3$, and $\mathrm{OSR} = 64$, (1) gives an upper bound of 118.9 dB, reduced in practice by finite OTA gain, thermal noise, jitter, switch nonlinearity, and quantizer error. The nominal OSR is 32 at a 1.6-MHz sampling frequency and 25-kHz bandwidth; following [8], double sampling doubles the effective rate to 3.2 MHz, giving $\mathrm{OSR}_{\mathrm{eff}} = 64$ without raising the clock frequency.

In an input-feedforward modulator the signal transfer function is ideally unity, giving

$$Y(z) = X(z) + \left(1 - z^{-1}\right)^3 E(z), \quad (2)$$

where $X(z)$ is the input, $E(z)$ the quantization noise, and $\left(1 - z^{-1}\right)^3$ the idealized third-order noise transfer function (NTF). The integrator outputs are therefore dominated by shaped quantization noise rather than by the full-scale input, which, with the 3-bit quantizer, reduces the required OTA output swing.

B. NTF Synthesis and Behavioral SNDR

The NTF was synthesized with the `synthesizeNTF` routine of the Schreier Delta-Sigma Toolbox [5] for $L = 3$, $\mathrm{OSR}_{\mathrm{eff}} = 64$, optimized zeros, and an out-of-band gain $\|H_\infty\| = 1.5$ (3.52 dB). All poles lie inside the unit circle and the in-band attenuation reaches approximately -70 dB; $\|H_\infty\|$ trades noise shaping against overload margin [5].

Fig. 2 shows the simulated SNDR versus input amplitude for a coherent sinusoid swept from -40 to 0 dBFS. The quantization-noise-only model reaches a peak SNDR of 83.5 dB at -2 dBFS (13.6 bits). Sweeping the order from one to four and the OSR from 16 to 128 at fixed quantizer resolution and out-of-band gain showed that lower values miss the 80 dB target while higher ones give only marginal gains at the cost of clock frequency, loop-filter complexity, and power; third order with $\mathrm{OSR}_{\mathrm{eff}} = 64$ is therefore the selected operating point.

A refined model adding sampled kT/C noise and input-referred OTA noise was then used. Its effective noise factor was calibrated against the 81.3-dB reference result [8] using ten independent noise realizations, then applied here with $C_s =$

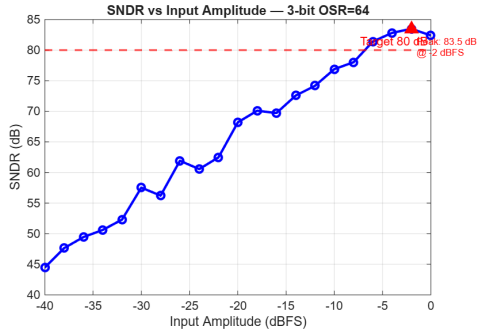

Fig. 2. Behavioral SNDR versus input amplitude ($\mathrm{OSR}_{\mathrm{eff}} = 64$, 3-bit quantizer). The peak SNDR of 83.5 dB occurs at -2 dBFS.

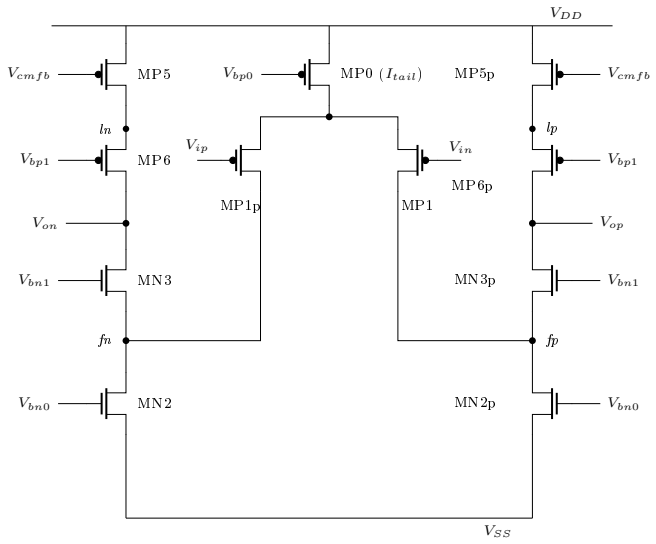

Fig. 3. Folded-cascode OTA core redrawn from the implemented schematic. MP1/MP1p form the PMOS differential input pair, MN3/MN3p the folded cascodes, and MP5/MP5p–MP6/MP6p the active load. The output nodes are V_{op} and V_{on}; V_{cmfb} is provided by the separate CT-CMFB cell.

125 fF and a 0.30-V differential full scale. The final evaluation uses a separate 20-realization set; results appear in Section IV-B.

III. Circuit-Level Design

A. Folded-Cascode OTA

The OTA sets the settling accuracy and linearity of the SC integrators. All three integrators use an identical fully differential folded-cascode OTA with a PMOS input pair and a resistive CT-CMFB circuit (Fig. 3). The folded-cascode replaces the telescopic OTA of the 180-nm design because at 1.0 V it gives greater output swing with fewer stacked devices and a wider input common-mode range [10]. A PMOS input pair was adopted for its lower flicker-noise coefficient, which matters in the 25-kHz band, and for more favorable biasing in the limited headroom.

The gain-bandwidth (GBW) requirement follows from the settling accuracy of the first integrator, which has the smallest feedback factor, $\beta_1 = 0.25$. For settling to an N-bit equivalent accuracy within half a clock period [10],

$$\mathrm{GBW}_{\min} = \frac{\mathrm{ENOB} \cdot \ln 2}{2\pi\, \beta_1\, (T_s/2)}, \tag{3}$$

Evaluated at the full system resolution, $\mathrm{ENOB} = 13.0$ bit with $T_s/2 = 312.5$ ns, (3) gives a worst-case requirement of 18.34 MHz. An SC integrator need not settle to the full converter resolution, however: it need only transfer charge accurately enough that incomplete settling does not dominate the system noise floor [10]. For this design, a 9-bit integrator-level settling criterion is adopted. On that criterion the first integrator requires $\mathrm{GBW} \approx 12.70$ MHz, against 13.47 MHz *calculated* from the extracted g_{m1} at its actual load $C_L = 455$ fF, a 5.7% settling margin. This is the binding constraint; the second and third stages ($\beta = 0.5$, $C_L = 205$ fF) have much larger margins. The input pair was sized to $g_{m1} = 38.51$ μS, giving

$$\mathrm{GBW} = \frac{g_{m1}}{2\pi C_L} = 12.26 \text{ MHz} \tag{4}$$

in hand calculation at the nominal $C_L = 500$ fF, while direct AC simulation gives 13.0 MHz at that load (Table I). This nominal half-cycle criterion is an integrator-level design check rather than proof of settling over the actual non-overlap clock window; the 5.7% margin remains a design risk assessed only functionally by transient simulation. Device dimensions were derived from DC operating-point parameters of the Cadence Generic 45-nm PDK (GPDK045), with channel lengths of 180–720 nm used across the OTA. Table I summarizes the simulated performance. The DC gain of 47.6 dB is below the long-channel hand-analysis prediction because of the short-channel reduction of r_o. The resistive CT-CMFB replaces the switched-capacitor CMFB of [8], avoiding the switch-threshold problem at 1.0 V at a static cost of about 0.5 μW per OTA.

Biasing: Four DC bias voltages and one feedback-generated voltage are required. V_{bp0} sets the tail current of MP0 to $I_{tail} = 2I_{D1} = 1.80$ μA. V_{bn0} biases MN2/MN2p, which carry $I_{D1} + I_{\mathrm{load}} = 1.152$ μA, making the folded branch current $I_{\mathrm{load}} = 0.252$ μA. The ratio $I_{\mathrm{load}}/I_{D1} = 0.28$ was chosen below the conventional 0.5 to raise the load output resistance and hence the DC gain; its lower bound follows from requiring $V_{ov,\mathrm{MP6}} \geq 40$ mV at the fast-fast corner, which yields 61.3 mV. V_{bn1} and V_{bp1} bias the cascodes at overdrives of 81.7 mV and 67.1 mV; under $\pm 20\%$ mobility variation the MN3 overdrive stays within 74.6–91.4 mV. Overdrives are held near 100 mV so the four stacked devices in each branch share 1.0 V while leaving the output free to swing. MP5/MP5p are driven by V_{cmfb} rather than a fixed bias; operating-point simulation gives $V_{cmfb} = 519$ mV with the output common-mode at 0.500 V.

In the simulations reported here, V_{bp0}, V_{bp1}, V_{bn1}, and V_{bn0} are applied as ideal DC voltage sources in the testbench. An on-chip bias generator, together with the voltage reference, V_{cm} buffer, and clock source, was not designed in this work and is identified as required future work; such a network will add area, static current, and process sensitivity not represented in the results below.

TABLE I
SIMULATED FOLDED-CASCODE OTA PERFORMANCE

Parameter	Value	Condition
DC gain A_{DM}	47.6 dB	Spectre, schematic
Gain-bandwidth, GBW	13.0 MHz	$C_L = 500$ fF
Phase margin	89.4°	$C_L = 500$ fF
Transconductance g_{m1}	38.51 μS	extracted (GPDK045)
Supply voltage	1.0 V	nominal
OTA core power	≈ 2.3 μW	nominal

B. SC Integrator and Sampling Capacitor

All three integrators use a parasitic-insensitive double-sampling SC topology following [8], with two sampling-capacitor sets operating alternately on the two clock phases. The first integrator uses $C_s/C_i = 1/3$ ($\beta_1 = 0.25$), the second and third $C_s/C_i = 1$ ($\beta = 0.5$). The sampled thermal-noise contribution is approximated by

$$\sigma^2_{\text{noise}} = \frac{kT}{C_s}, \tag{5}$$

where k is Boltzmann's constant and T the absolute temperature. A direct single-sample interpretation would imply an impractically large capacitance, but sampled input-referred noise is averaged by oversampling rather than shaped by the NTF. For $\text{OSR}_{\text{eff}} = 64$, the corresponding averaging term is approximately $10\log_{10}(64) = 18$ dB [5]. Accordingly, $C_s = 125$ fF was adopted as a design choice consistent with [8] and evaluated in the calibrated noise model of Section IV-B rather than claimed as a first-principles minimum.

C. Bootstrapped Switch

At $V_{DD} = 1.0$ V an NMOS switch carrying a mid-supply signal has $V_{GS} = 0.5$ V, below $V_{th,N} = 0.588$ V, and cannot turn on; a transmission gate also fails because $|V_{th,P}| = 0.574$ V leaves negative PMOS overdrive at mid-range [11]. The Dessouky–Kaiser bootstrapped switch [11] of Fig. 4 pre-charges a bootstrap capacitor $C_{\text{offset}} = 50$ fF to V_{DD} and connects it between gate and source during the on-phase, such that

$$V_{GS,\text{MNSW}} \approx V_{C_{\text{offset}}} \approx V_{DD} \tag{6}$$

independently of the input signal. For a minimum-width main switch ($W_{\text{MNSW}} = 120$ nm) the on-resistance is $R_{on} = 2.57$ kΩ, well below the settling-time limit, and the nearly constant overdrive strongly reduces the signal-dependent modulation of R_{on}, improving linearity.

D. Resistive DAC, Comparator, and Clock Generator

The 3-bit feedback DAC produces eight reference levels from a resistor string with $R_u = 10$ kΩ, implemented as two identical strings for the complementary differential outputs. Fig. 5 shows one string as implemented: eight unit resistors R01–R78 form a chain of nine nodes between the external ports V_{bot} and V_{top}, and eight low-V_{th} NMOS pass switches ($W/L = 2.0$ μm/180 nm, $R_{on} = 517$ Ω) connect the lower eight nodes to the common output, the top node V_{top} being unselected. The selected levels are therefore separated by one

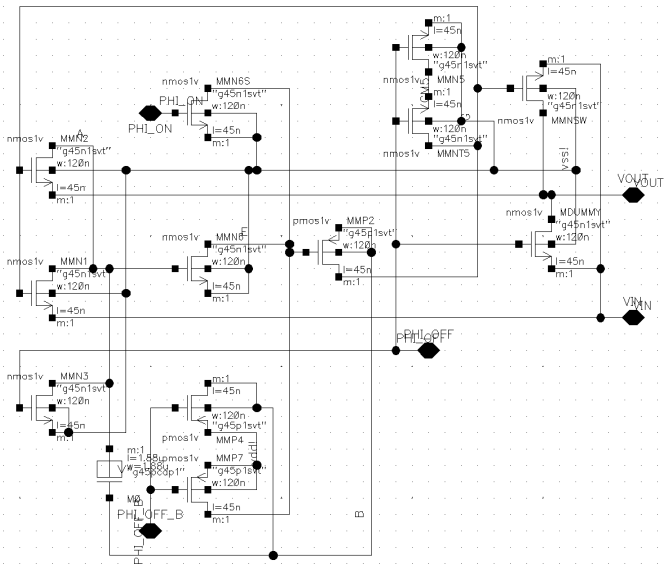

Fig. 4. Implemented Dessouky–Kaiser bootstrapped switch [11], shown from the final schematic. The bootstrap capacitor C_{offset} maintains $V_{GS,\text{MNSW}} \approx V_{DD}$ across the input range.

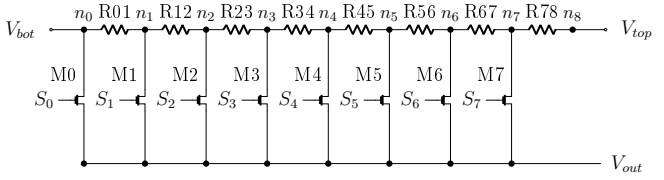

Fig. 5. Implemented 3-bit resistor-string feedback DAC (one of two identical differential strings). Eight 10-kΩ unit resistors form nodes n_0–n_8; switches M0–M7 select n_0–n_7 to V_{out}, while $n_8 = V_{top}$ remains unselected.

unit resistor each, spanning seven unit drops. Operating-point simulation gives 0.250, 0.3125, 0.375, 0.4375, 0.500, 0.5625, 0.625, and 0.6875 V, a uniform 62.5-mV step over a 437.5-mV single-ended range, consistent with this topology. With complementary tap selection the differential feedback range is ± 437.5 mV and the differential LSB is 125 mV.

These levels differ from the design target of 0.325–0.675 V in 50-mV steps used to set the flash thresholds. The intended design assumed a seven-segment chain with both endpoints selectable; the implemented string has an eighth resistor above the highest selected node, making the step one eighth of the V_{bot}–V_{top} span rather than one seventh. The operating-point levels and eight-segment topology correspond to $V_{bot} = 0.250$ V and $V_{top} = 0.750$ V in the reported testbench. The ladder itself remains uniform and monotonic; to first order, the resulting $+25\%$ scaling error acts primarily as a feedback-gain and full-scale mismatch, but its complete closed-loop dynamic impact was not characterized. The feedback common-mode level is also 468.75 mV instead of 500 mV; this offset must be accommodated by the CMFB loop and consumes available common-mode headroom. Each 80-kΩ string therefore draws 6.25 μA and dissipates 3.125 μW from the external reference rails; the two differential strings dissipate 6.25 μW in total, excluding the overhead of generating and buffering V_{top} and

V_{bot}. Matching the flash thresholds to the implemented levels is left as a correction for the next iteration. DAC errors enter the loop directly and are not shaped by the NTF [5].

The 3-bit flash quantizer uses seven dynamic latch comparators [13]; Pelgrom-based sizing [14] targets input-referred offset below LSB/2, but a full mismatch Monte Carlo is outside the present verification. A NAND-based four-phase non-overlapping clock generator produces θ_1, θ_{1d}, θ_2, and θ_{2d} for bottom-plate sampling.

IV. Results and Discussion

A. OTA Performance and Gain Sensitivity

Transistor-level DC and AC simulation gives $A_{DM} = 47.6$ dB, GBW $= 13.0$ MHz, and a phase margin of $89.4°$ (Table I). A separate simplified behavioral sensitivity sweep models finite OTA gain only as integrator leakage. Within that leakage-only model, degradation becomes pronounced as the gain approaches the mid-30-dB range, consistent with the guideline $A_{DM} \gtrsim \text{OSR}$, or $20\log_{10}(64) \approx 36$ dB [5]. Because this sweep uses a different simplified model from both the quantization-noise-only optimization and the calibrated noise-included evaluation, its absolute SNDR values are not compared directly with those results. It supports only the qualitative conclusion that finite gain at the achieved 47.6 dB is not by itself the dominant modeled limitation; the sweep is not a transistor-level dynamic-performance proof.

B. Output Spectrum and Resolution

Fig. 6 shows the noise-included behavioral output magnitude spectrum. The exact third-order NTF uses optimized zeros with $\|H_\infty\| = 1.5$. Its effective noise factor is calibrated against the 81.3-dB reference [8] over ten noise realizations; the present design is then evaluated with 20 separate realizations.

The effective sampling rate is $f_{s,\text{eff}} = 3.2$ MHz, $N_{\text{FFT}} = 65\,536$, and a periodic Hann window is used, giving 48.83-Hz bin spacing and a 25-kHz band edge at bin 512. A -2 dBFS coherent input is placed at bin 67, $f_{in} = 3.271484375$ kHz; HD2–HD7 therefore lie from 6.543 to 22.900 kHz and remain in band. DC is excluded, the five-bin Hann main lobe around the fundamental is treated as signal, and every other in-band bin, including harmonics, is counted as noise plus distortion. Across the 20 evaluation realizations, the mean SNDR is 78.38 ± 0.23 dB (range 78.05–78.81 dB). From

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02}, \tag{7}$$

the mean ENOB is 12.73 bit. The behavioral ENOB remains above 12 bits, consistent with the adopted ECG-oriented design benchmark, but misses the more stringent 80-dB design target by 1.62 dB. The model includes quantization noise, calibrated sampled/OTA-noise contribution, and simplified finite-gain leakage; it does not establish transistor-level FFT SNDR or include OTA large-signal distortion, switch nonlinearity, DAC mismatch, parasitic extraction, or Monte Carlo variability.

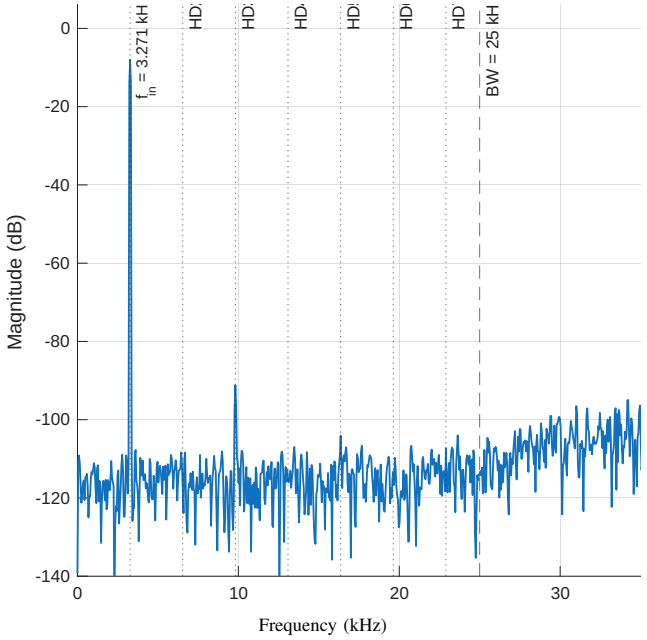

Fig. 6. Noise-included behavioral output spectrum for the coherent 3.271-kHz input. HD2–HD7 remain inside the 25-kHz band. The plotted representative realization (seed 26) gives 78.34-dB SNDR and 12.72-bit ENOB; the 20-realization mean is 78.38 ± 0.23 dB.

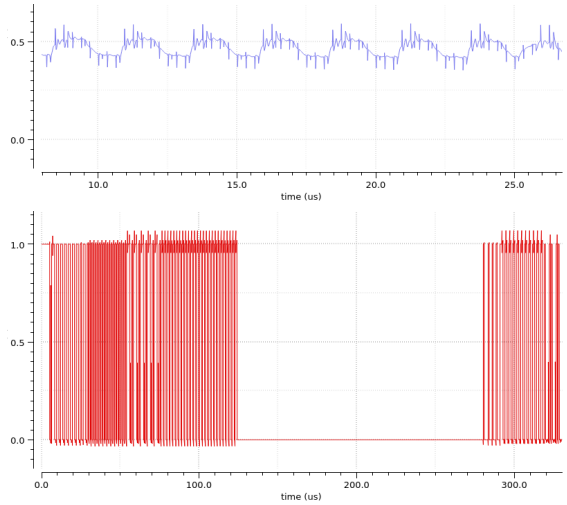

Fig. 7. Closed-loop transistor-level transient simulation (vertical axes in volts). Top: first-integrator output V_{1p} under a sinusoidal input, 7–27 μs detail, bounded about the common-mode level. Bottom: quantizer output bit B_0 over the full 330-μs interval, showing the pulse-density variation that follows the input envelope.

C. Closed-Loop Verification

The modulator was verified by closed-loop transient simulation, built up incrementally from a first-order to the full third-order configuration. Under zero differential input the average quantizer output remains near mid-code, confirming correct loop biasing. Throughout the simulation interval, all integrator outputs remain bounded and the loop is stable without divergence or overload. Fig. 7 shows the first-integrator output tracking the input envelope and the quantizer bit exhibiting the expected pulse-density behavior.

TABLE II
PERFORMANCE COMPARISON WITH PUBLISHED $\Sigma\Delta$ MODULATORS

Ref.	Tech. (nm)	V_{DD} (V)	Power (μW)	SNDR (dB)	FoM (fJ)
[15]	90	0.2	0.44	44.2	57
[7]	130	0.6	28.6	79.1	97
[16]	180	1.8	280	98.9[b]	88
[17]	180	1.8	90	93.5[c]	48[c]
[8]	180	1.8	28.2[e]	81.3[e]	59
This work	**45**	**1.0**	**46.25**[a]	**78.38**[d]	**136.37**[f]

[a]Modeled subtotal: ≈ 40 μW V_{DD} core + 6.25 μW passive DAC ladders; excludes bias/reference-generator overhead and layout parasitics. $\mathrm{BW} = 25$ kHz, $\mathrm{OSR}_{\mathrm{eff}} = 64$. [b]Raw SNR over a 24-kHz bandwidth. [c]Dynamic range over a 24-kHz bandwidth; FoM computed from this DR. [d]Noise-included behavioral estimate. [e]Post-layout simulation. [f]Projected from the modeled power subtotal and behavioral ENOB.

D. Power Consumption and Figure of Merit

Closed-loop Spectre transient simulation gives approximately 40 μW of V_{DD}-powered modulator-core power. The passive DAC ladders are supplied instead from the external reference rails and therefore are not included in that V_{DD} current; as derived in Section III-D, the two strings dissipate an additional 6.25 μW. The modeled subtotal is therefore approximately 46.25 μW before on-chip bias/reference generation, pads/ESD, decimation, and layout parasitics. This subtotal is below the original 50-μW target, but it does not establish full-chip power compliance because the omitted bias/reference-generator overhead was not designed or measured. Table II reports this modeled subtotal.

The energy efficiency is evaluated using the Walden FoM [18],

$$\mathrm{FoM} = \frac{P}{2^{\mathrm{ENOB}} \cdot 2\,\mathrm{BW}}, \tag{8}$$

Using $P \approx 46.25$ μW, $\mathrm{BW} = 25$ kHz, and the 12.73-bit behavioral ENOB gives 136.37 fJ/conversion-step. This is a *projected* FoM because it combines a schematic-level modeled power subtotal with behavioral ENOB; the revised estimate does not meet the original < 100-fJ design target.

E. Comparison with Prior Work

Table II compares this design with the 180-nm reference [8] and other reported low-power $\Sigma\Delta$ modulators. The GBW of 13.0 MHz is approximately $3.6\times$ that of [8] (3.64 MHz). This work's 46.25-μW value is a schematic-level modeled subtotal (including passive ladder dissipation but excluding bias/reference-generator overhead), and its 78.38-dB SNDR is behavioral; several references report post-layout or differently defined dynamic metrics, so the table is contextual rather than an apples-to-apples ranking.

V. CONCLUSION

This work redesigns a third-order feedforward 3-bit $\Sigma\Delta$ modulator using the Cadence Generic 45-nm CMOS PDK at 1.0 V, with a folded-cascode OTA, Dessouky–Kaiser bootstrapped switches, and resistive CT-CMFB. The quantization-noise-only model reaches 83.5-dB peak SNDR, while the revised noise-included behavioral evaluation with a 3.271-kHz coherent tone gives 78.38 ± 0.23 dB and 12.73-bit ENOB. The behavioral ENOB remains above 12 bits, consistent with the adopted ECG-oriented design benchmark, but the more stringent 80-dB design target is missed by 1.62 dB. Closed-loop schematic-level transistor simulation gives approximately 40 μW of V_{DD}-powered core power; including 6.25 μW of passive DAC-ladder dissipation yields a modeled subtotal of 46.25 μW before on-chip bias/reference-generator overhead. Combining this subtotal with behavioral ENOB gives a projected Walden FoM of 136.37 fJ/conversion-step, above the original 100-fJ target. The finite-gain sensitivity study indicates qualitatively that the achieved 47.6-dB OTA gain is not by itself the dominant modeled limitation. Full transistor-level spectral verification, bias/reference integration, flash-threshold rematching, clock-settling optimization, parasitic extraction, process/mismatch variability analysis, and complete physical verification remain future work.

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